

FIG. 1A

The diagram shows a current source 180. It consists of a differential pair of PMOS transistors 184 and 124. The gates of these transistors are connected to a common gate voltage. The sources of both transistors are connected to a common source node, which is connected to ground 170 through a resistor 120. A current source 122, controlled by a signal 'CONTROL' with gain 'n', is connected in parallel with resistor 120. The drains of transistors 184 and 124 are connected to a supply voltage 182 through a resistor 110. A current mirror 150 is connected to the drain of transistor 184, with its input connected to the drain of transistor 124. The output of the current mirror 150 is connected to a load resistor 112. A reference current I_{REF} is shown flowing into the source node. The circuit is powered by a supply voltage 182 and a reference current I_{REF} .



TITLE: CURRENT REFERENCE BASED ON A KNOWN RESISTANCE VALUE
INVENTORS NAME: James E. Jaussi et al.
SERIAL NO.: 09/995,013

3/6

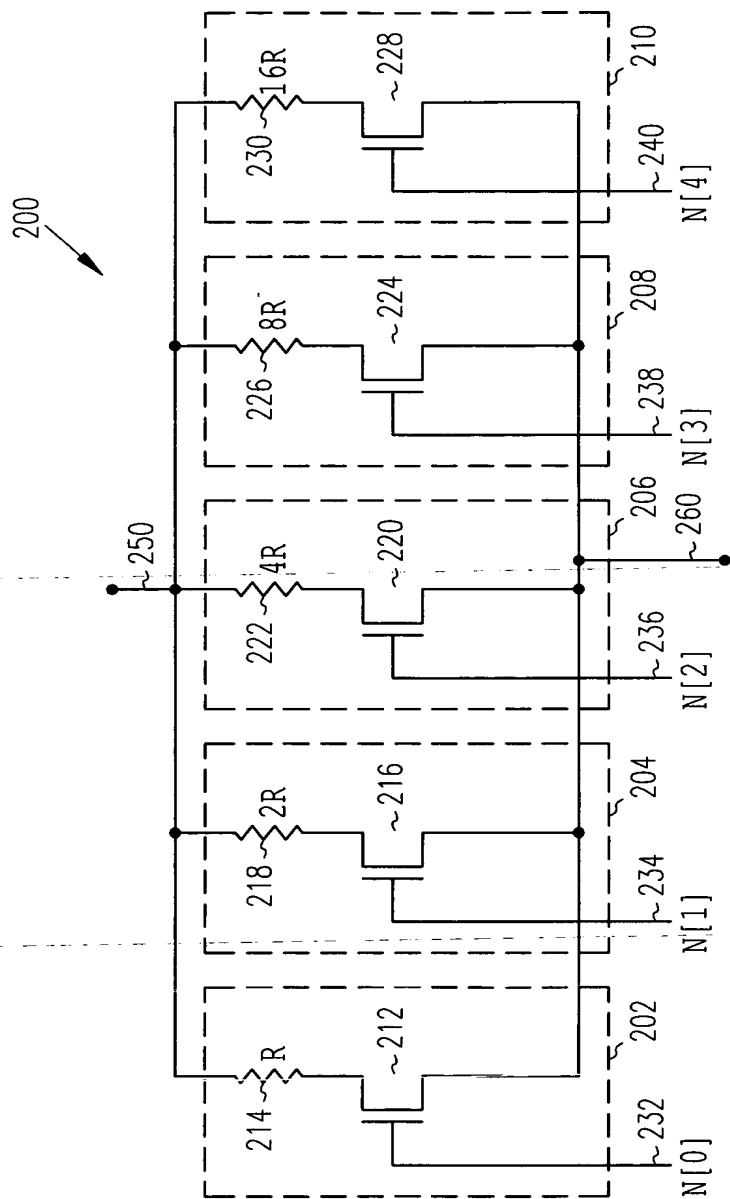


FIG. 2

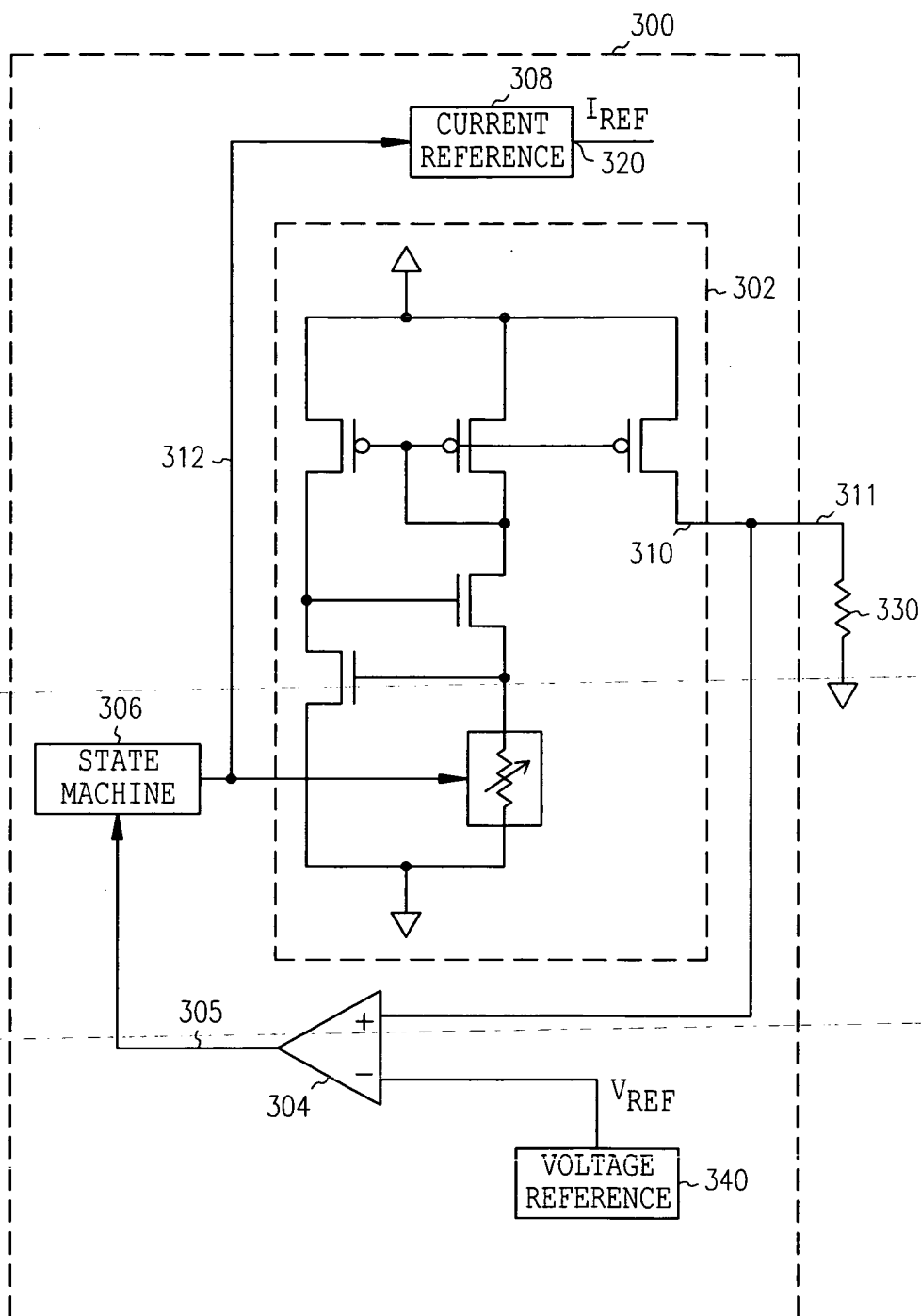


FIG. 3

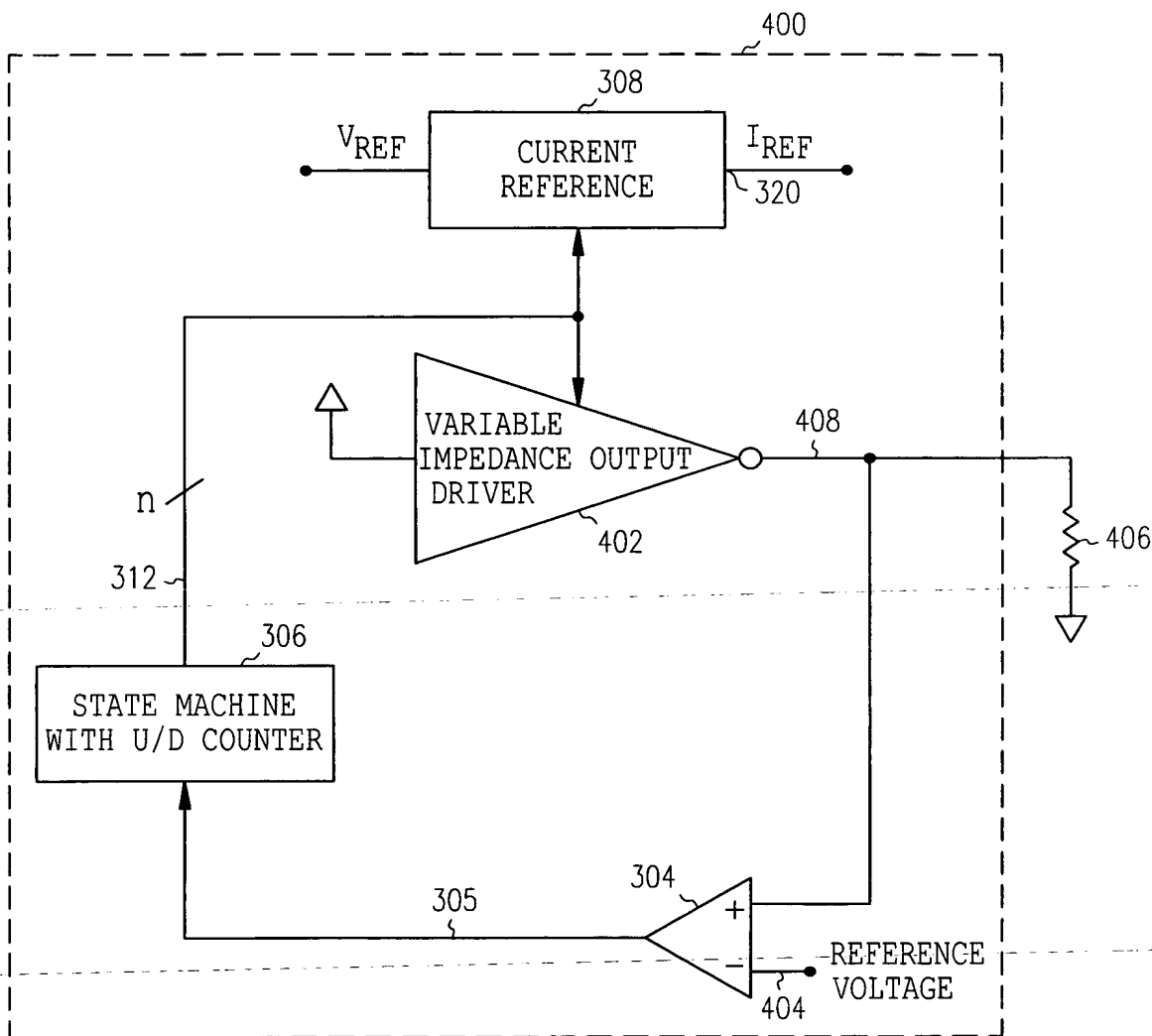


FIG. 4

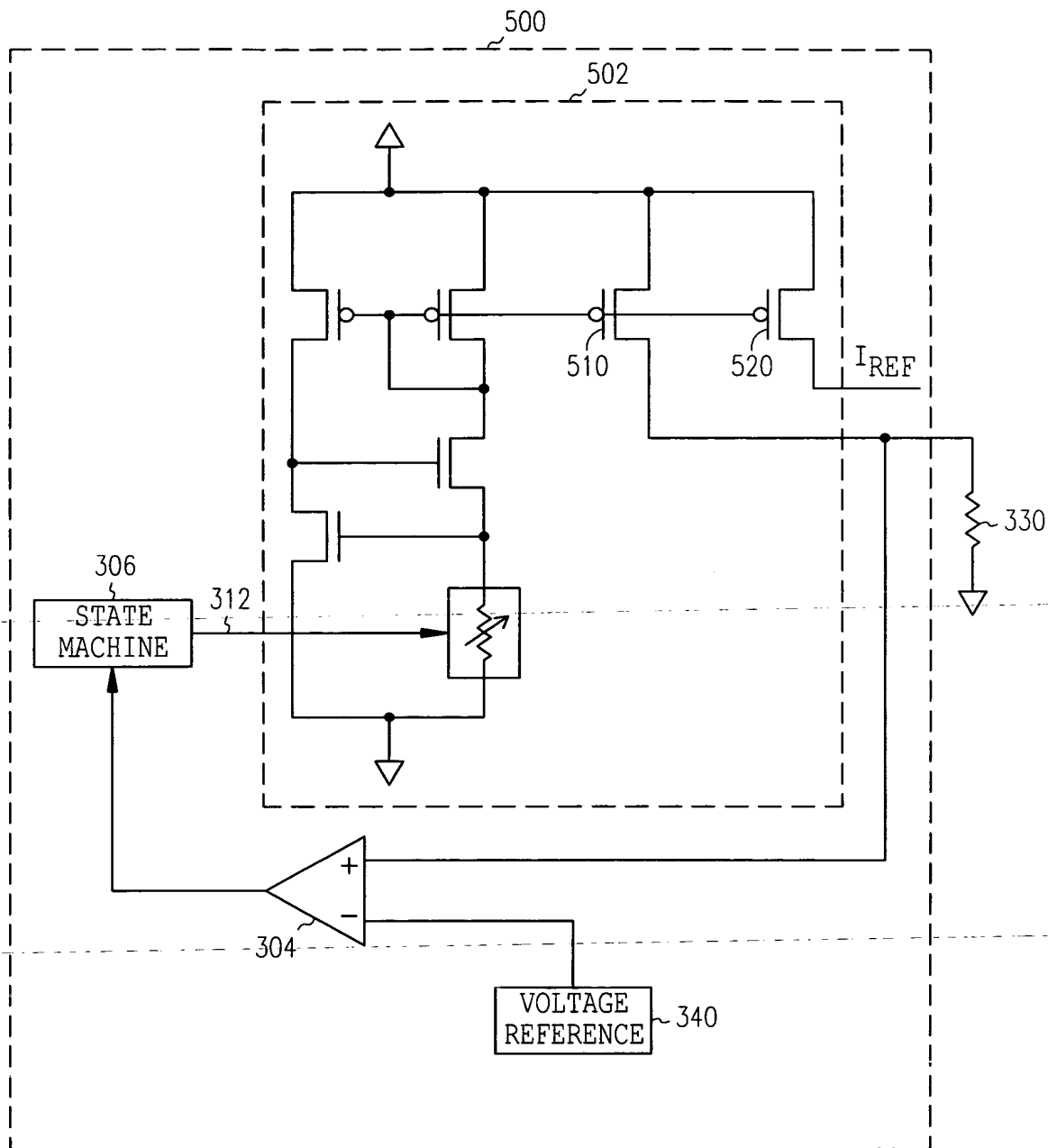


FIG. 5